Small-Signal and Power Evaluation of Novel BiCMOS-Compatible Short-Channel LDMOS Technology

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***Abstract*—We describe a very short-channel 0.15-μm LDMOS transistor with a breakdown voltage of up to 60 V, manufactured in a standard 0.35-μm BiCMOS process. At 1900 MHz and a 12-V supply voltage, the 0.4-mm-gatewidth device with shortest drain drift region gives 100-mW output power $P_{1\,\mathrm{dB}}$ at a drain efficiency of 43%. It has a transducer power gain of over 20 dB. The maximum current gain cutoff frequency f_T is 15 GHz, and the maximum available gain cutoff frequency f_{MAX} is 38 GHz. We show the dependence of f_T, an f_{MAX} of gate and drain bias for transistors with different drain drift region length. The LDMOS process module does not affect the performance or the models of other devices. We present for the first time a simple way to create high-voltage high-performance LDMOS transistors for an RF power amplifier use even in a very downscaled silicon technology.**

***Index Terms*—BiCMOS integrated circuits, high-frequency (HF) amplifiers, LDMOS, microwave power FETs, MOSFET power amplifiers (PAs).**

I. Introduction

THE ever-increasing market for digital base-station power amplifiers (PAs) in personal communications system (PCS), CDMA, and WCDMA systems requires low-cost ease-of-use technology, which can provide high-power and good linearity performance. LDMOS started replacing bipolar devices in base-station applications 3–4 years ago and has, for multiple reasons, become the leading technology for base-station PA applications. It has high gain and shows excellent backoff linearity [1]. The breakdown voltage $\mathrm{BV_{dss}}$ can be easily adjusted by layout to fit different application voltages. The integration of LDMOS transistors into an RF BiCMOS process [2], [3], including the necessary passive components, provides a tool for design of monolithic silicon amplifiers with sensing and control circuitry on-board. More importantly, it also opens the way to more efficient linear RF PAs with integrated linearization circuits on the same die. The output power of such an integrated PA should be in the 10-W range, with a power supply of 10–12 V, requiring LDMOS transistors with a breakdown voltage higher than 30 V. This paper describes a very short-channel high-performance LDMOS structure, which is simple to integrate with conventional CMOS/BiCMOS and does not affect other devices, its processing, dc, and ac performance. It also presents an evaluation of different drain drift regions for the device.

Manuscript received September 6, 2002.

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Digital Object Identifier 10.1109/TMTT.2003.808697

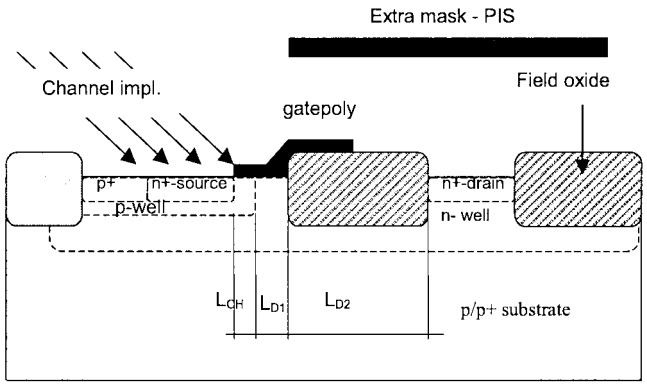

Fig. 1. LDMOS device structure dimensions after processing: $L_{\mathrm{CH}} = 0.15\ \mu$m, $L_{D1} = 0.15\ \mu$m, $L_{D2} = 1.2$–$2.4\ \mu$m (different layouts).

II. Device Design and Fabrication

The LDMOS transistor was implemented in a standard 0.35-μm BiCMOS process adapted for RF applications. The LDMOS process required only one extra implantation mask, with no additional heat treatment, thus, not affecting the performance and models of other devices. The implantation was performed as a pocket implant [4] of boron at an angle of 30° to provide the necessary LDMOS p-well (p-body) surrounding the source diffusion (see Fig. 1) for transistor structure.

The resulting channel length of the transistor was approximately 0.15 μm according to Athena process simulation. The gate oxide in the channel region was the same as for the other CMOS transistors, i.e., 6.7 nm. The bird's beak encroachment from the field oxide covering the extended drain was approximately 0.1 μm (see transistor cross section in Fig. 2), leaving only the distance of 0.3 μm between the gate edge and thick field oxide. The process used Ti salicide to reduce the series resistance on both polysilicon gates and source/drain areas, but also to strap the source n+ diffusion to the p+ body contact. The process has an option of deep metal plugs that make it possible to strap the source regions of the LDMOS transistors to a p+ substrate [5]. The transistor layout was optimized for both high-voltage and high-frequency (HF) performance. The transistors were designed as multifinger devices with 20-μm gatewidth of each finger. The drain was enclosed by the gate

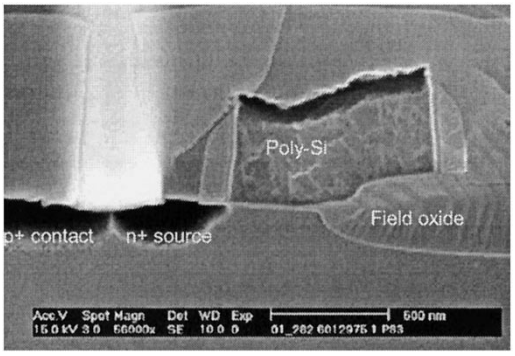

Fig. 2. LDMOS transistor cross section from the source side.

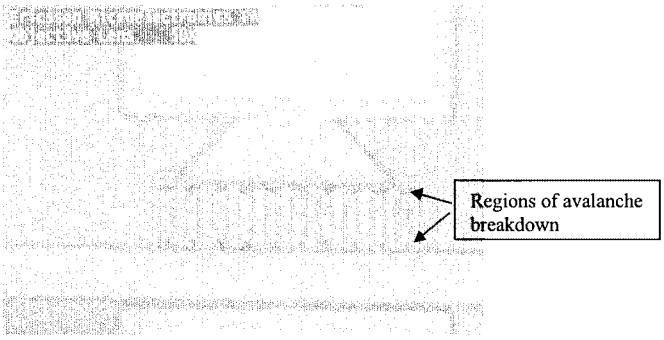

Fig. 3. Emission micrograph of the transistor showing the avalanche breakdown at the end of the drain fingers.

to minimize both $C_{\rm ds}$ and to avoid fringing fields, reducing the breakdown voltage. The extended drain region, separating the channel region from the drain contact, was covered by thick field oxide, reducing both $C_{\rm gd}$ and significantly increasing the possible $V_{\rm gd}$ before oxide breakdown.

III. DC Performance

Transistors were manufactured with three different extended drain regions: 1, 1.5, and 2.2 μm (mask dimension). The breakdown voltage $\rm BV_{ds}$ is approximately 35, 40, and 45 V, respectively. The breakdown is limited by the high field at the corners of the drain region, observed by emission microscopy (Fig. 3).

Transistors with adjusted gate–drain field plate layout, recently manufactured, showed an increased breakdown voltage of 40, 50, and 60 V for the above described transistors (see Fig. 4). The evaluation of the new transistors will be the subject of future studies. The series resistance $R_{\rm ds}$ in the linear region of the *I–V* characteristics is also affected by the size of extended drain region, varying by almost a factor of two for the shortest and longest device. The maximum available drain current $I_{\rm ds}$ is over 50 mA at a $V_{\rm gs}$ of 3.5 V for the devices with 0.4-mm total gatewidth and almost independent of the length of the extended drain region. Since the transistors with the extended drain region of 1 μm have high enough breakdown voltage for the application, the following power data address these devices. An example of the *I–V* characteristics of the transistor are presented in Fig. 5.

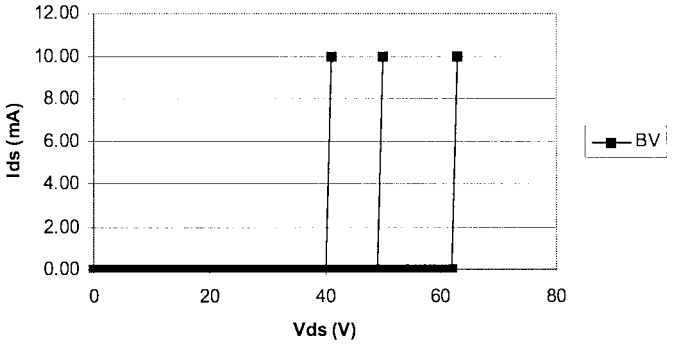

Fig. 4. Breakdown voltage, from left to right, for transistors with drain length 1, 1.5, and 2.2 μm, respectively.

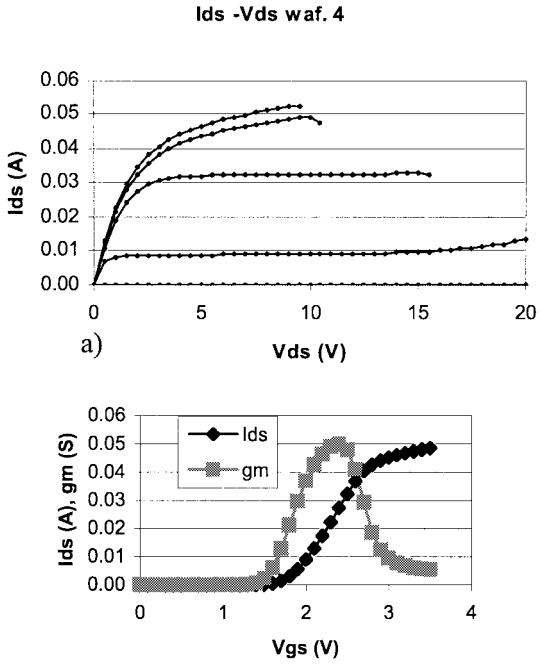

Fig. 5. *I–V* characteristics of LDMOS transistor with a total gatewidth of 0.4 mm, and extended drain region of 1 μm. (a) $I_{\rm ds}$ versus $V_{\rm ds}$ for $V_{\rm gs}$ = 1–3.5 V in 0.5-V steps. (b) $I_{\rm ds}$ and g_m versus $V_{\rm gs}$ at $V_{\rm ds}$ = 6 V, $V_{\rm th}$ = 1.8 V.

IV. Small-Signal AC Performance

Small-signal s-parameters were measured on wafer with a standard 150-μm pitch ground–signal–ground probe calibrated and deembedded for pad capacitances. The current gain h_{21} was calculated and the current gain cutoff frequency f_T was extracted for different drain voltages and drain drift regions. Maximum f_T was found to be 15 GHz for the shortest device at lowest supply voltage, i.e., 6-V dc. The maximum available gain cutoff frequency $f_{\rm MAX}$ = 38 GHz was extrapolated from the MAG measurements (Fig. 6) at the highest voltage, i.e., 15-V dc and 18-mA drain current. The bias dependence of f_T and $f_{\rm MAX}$ is shown in Figs. 7–9.

As can be seen, bias has a large influence on both f_T and $f_{\rm MAX}$ due to g_m compression and the bias dependence of the input capacitance, denoted here as C_g. To separate the influence

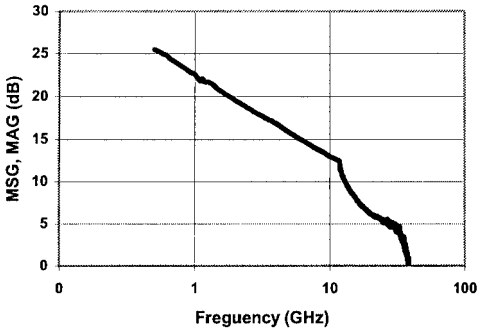

Fig. 6. Small-signal MSG and MAG versus frequency at 15-V dc supply voltage and 18-mA drain current.

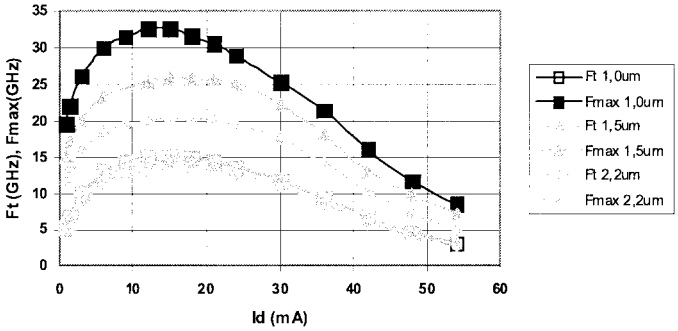

Fig. 7. Current gain and maximum available gain cutoff frequencies versus drain current at 6-V dc supply voltage for different drain drift region lengths.

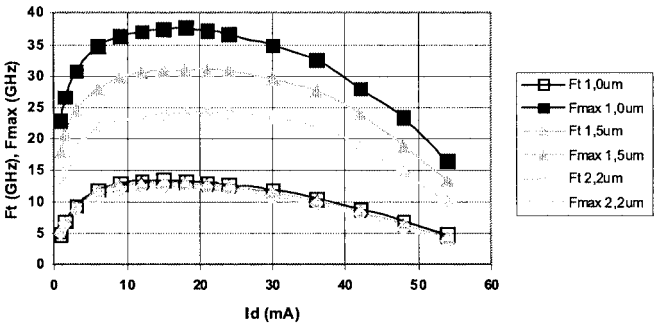

Fig. 8. Current gain and maximum available gain cutoff frequencies versus drain current at 12-V dc supply voltage for different drain drift region lengths.

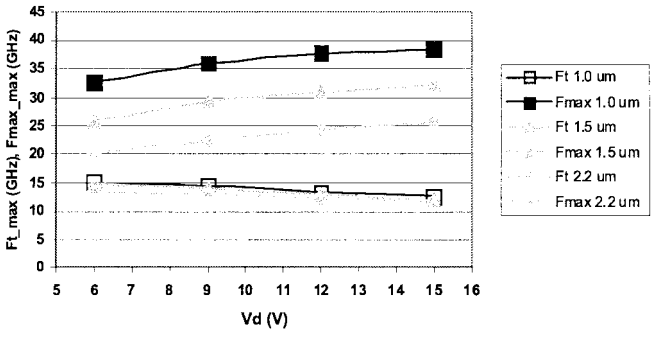

Fig. 9. Maximum current gain cutoff frequency and maximum available gain cutoff frequencies versus drain voltage for different drain drift region lengths.

of these mechanisms, the input capacitance was calculated using the following equation [6] and is plotted in Figs. 10–12:

$$\omega_T = \frac{g_m}{C_g}, \qquad \text{where } \omega_T = 2 * \pi * f_T.$$

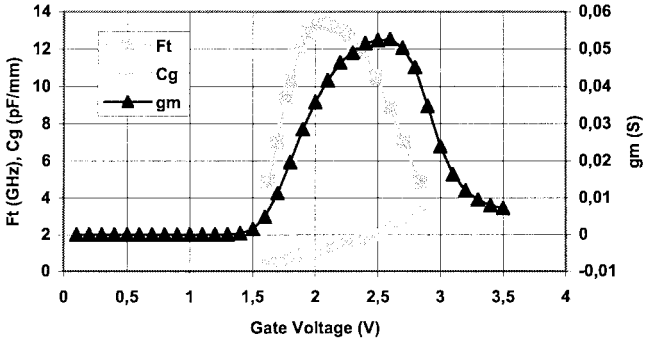

Fig. 10. Current gain cutoff frequency, transconductance, and calculated input capacitance versus gate voltage for 0.4-mm gatewidth and 1.0-μm drift region measured at a drain voltage of 12 V.

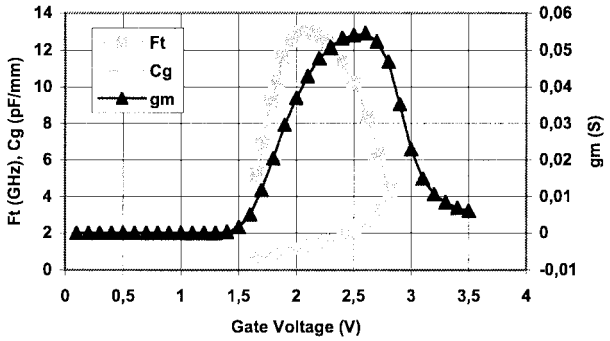

Fig. 11. Current gain cutoff frequency, transconductance, and calculated input capacitance versus gate voltage for 0.4-mm gatewidth and 1.5-μm drift region measured at a drain voltage of 12 V.

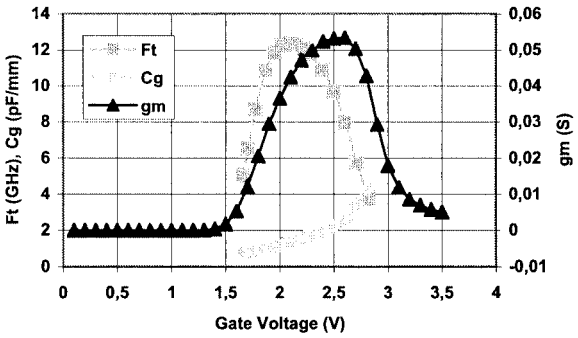

Fig. 12. Current gain cutoff frequency, transconductance, and calculated input capacitance versus gate voltage for 0.4-mm gatewidth and 2.2-μm drift region measured at a drain voltage of 12 V.

From Figs. 10–12, it is clearly shown that the major contributor to the f_T rolloff with gate bias is the bias dependence of the input capacitance. Comparing the capacitance value to the oxide capacitance C_{ox} (approximately 1.53 pF/mm) shows that the input capacitance for high gate voltage can be up to three times C_{ox}, as shown by [7]–[9]. The drain drift region length has a small influence on C_g, as shown in Fig. 13. Together with the small difference in g_m, it accounts for the differences in f_T of approximately 10% for the devices with different drain drift region length. The drain drift region length has, however, a large impact on f_{MAX}. An increase of drain drift region from 1.0 to 2.2 μm gives nearly a 40% reduction of f_{MAX} (Figs. 7 and 8). This is mainly caused by the increased drift region resistance causing an increased drain resistance R_D directly af-

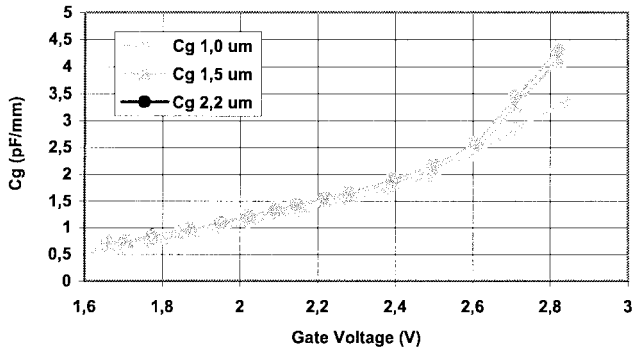

Fig. 13. Input capacitance C_g for a different length of drift region versus gate voltage measured at a drain voltage of 12 V.

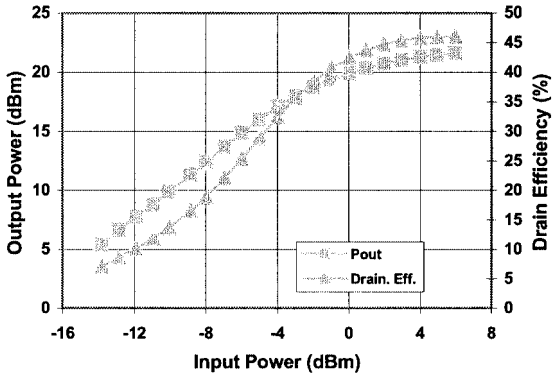

Fig. 14. Output power and drain efficiency versus input power at 1.9 GHz, 12-V dc supply voltage, and 3-mA quiescent drain current.

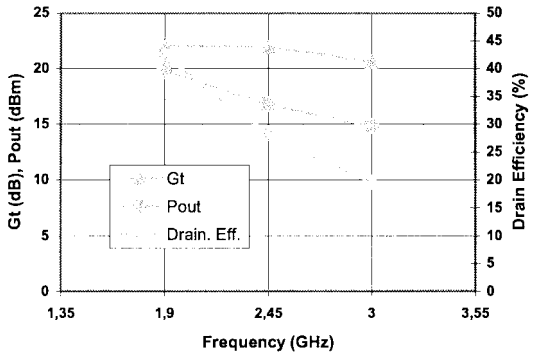

Fig. 15. Gain, output power, and drain efficiency at the 1-dB compression point versus frequency for 12-V dc supply voltage and 3-mA quiescent drain current.

fecting f_{MAX} [10]. Figs. 7–9 also show that maximum f_{MAX} increases considerable with supply voltage, while maximum f_T decreases somewhat. This is mainly due to the reduction of output capacitance C_{OUT} with increasing V_D, as shown in [10].

V. Power Performance

Power evaluation was made using a Maury Automated Tuner System (ATS) at the probe interface with probe tips calibrated using a standard calibration substrate. No deembedding was done. Single-tone excitation at 1.9 GHz shows very high transducer power gain G_t of over 20 dB and a reasonable output power of 100 mW (20 dBm) at the 1-dB compression point. The drain efficiency at that point is 43% and reaches a maximum of 46% further into compression (Fig. 14).

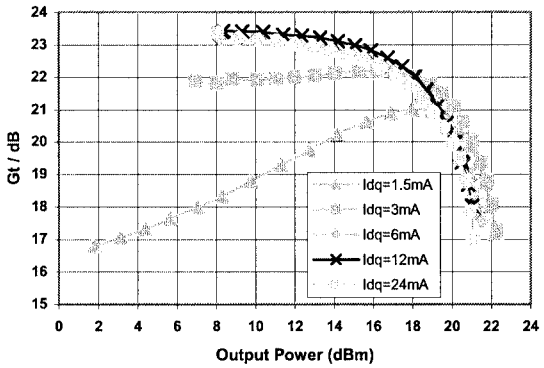

Fig. 16. Gain versus output power and quiescent drain current at 1.9 GHz and 12-V dc supply voltage.

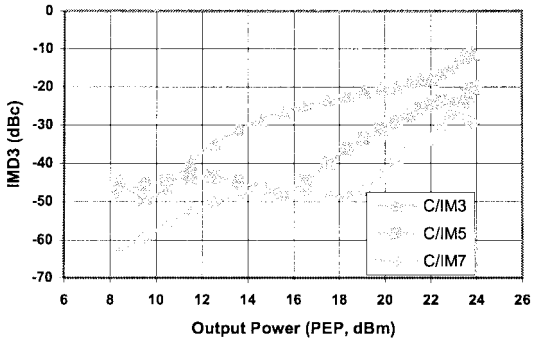

Fig. 17. Two-tone IMD versus PEP at 12-V dc supply voltage and 3-mA quiescent drain current. $f_1 = 1.9000$ GHz. $f_2 = 1.9001$ GHz.

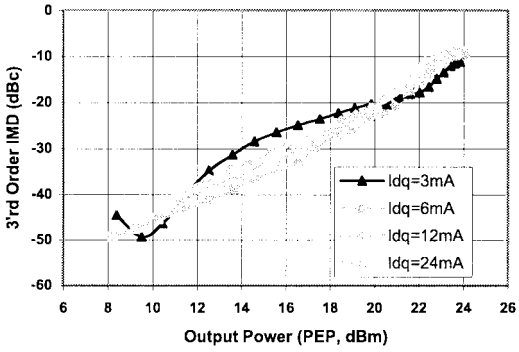

Fig. 18. Two-tone IMD3 versus peak envelop output power for different bias points at 12-V dc supply voltage. $f_1 = 1.9000$ GHz. $f_2 = 1.9001$ GHz.

The device also shows high power gain for higher frequencies (Fig. 15), which is in line with the low rolloff rate of the small-signal MSG, -10 dB per decade until the breakpoint is reached [9], [11]. At 3.0 GHz, the device still shows an extremely high transducer power gain of over 20 dB, but the drain efficiency has gone down to 20% with an output power of 30 mW (15 dBm) at the 1-dB compression point. The gain is very bias dependent, as shown in Fig. 16, as can be expected from the bias dependence of f_{MAX} shown in Fig. 8. The graph shows a maximally flat gain at a quiescent drain current of 3 mA, a low-class AB bias point. The 1-dB output power compression point increases from 17 to 19 dBm going from class A to class AB, but at the expense of approximately 2-dB lower gain, as expected [12].

VI. Two-Tone Power Performance

Evaluation of two-tone intermodulation distortion (IMD) was performed in the same measurement setup as shown in Section V. The measurement results of the device at 1.9 GHz are shown in Figs. 17 and 18. For the maximally flat gain, at a quiescent drain current of 3 mA, the third-order intermodulation distortion (IMD3) is −20 dBc at a peak envelope output power (PEP) of 21 dBm (Fig. 17). When backed off to third-order IMD, less than −30 dBc, the PEP output drops to 17.5 dBm at the optimum bias of 6 mA (Fig. 18).

The IMD3 values versus bias show a substantial bias sensitivity resulting in a maximum difference of over 10 dB in the backed-off region often used in modern telecommunications systems with high peak to average ratio.

VII. Conclusion

We have described and evaluated an HF high-voltage LDMOS transistor incorporated in a standard CMOS/BiCMOS process. Since this addition does not affect the performance of other devices, the reuse of old design blocks is possible without any major changes. The measured RF-power and distortion behavior meet the requirements for integrated PAs for a supply voltage of 10–12 V. The results also indicate that operation could be extended up to a few gigahertz range, which is the subject of current investigations. The on-wafer measurements cannot be directly compared to the demands placed on packaged devices by modern communication standards and designed for higher supply voltage [13]. The measurement results show higher gain and reduced IMD performance in comparison to packaged transistors with internal matching.

Acknowledgment

The authors wish to acknowledge Ericsson Radio Access AB, Kista, Sweden, and especially Z. Draganic for fruitful measurement discussions and for making the power measurements possible at their facilities. The authors would also like to acknowledge Agilent-EEsof, Kista, Sweden, for donating software used within this study.

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Jörgen Olsson (S'93–M'96) was born in Uddevalla, Sweden, in 1966. He received a University Certificate in electronics and the Ph.D. degree in electronics from Uppsala University, Uppsala, Sweden, in 1990 and 1996, respectively.

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